Dynamic Stress Analysis of TSOP Devices with Different Chip Sizes

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1. INTRODUCTION

Thin-Small-Outline-Plastic (TSOP) encapsulated electronic devices are becoming more and more popular in spaceborne electronic systems largely because of their high density, light weight, and low profile. This package allows PCBs to be fabricated smaller, lighter, and thinner than standard TSOPs, thereby making the PCB assesmbly more vibration-resistant. Our previous study on TSOP devices also concluded that TSOP devices have better thermal characteristics than that of PEMs with thicker plastic molding compound material [1]. Recent industrial trends show that new TSOP devices are made with a very thin molding compound and with a relatively large silicon chip. However, when the molding compound gets thinner and the chip size gets relatively larger, dynamic stresses on the silicon material are expected to be different form that of the regular devices where the chip size is relatively very small. Since all of the NASA spaceborne PCB assemblies will have to go through stringent random vibration testing, understanding the dynamic stress distribution on large chips in TSOP packages will give us good insight when selecting ultra-thin TSOP devices for electronic system operating under severe dynamic environment.

This study uses TOSHIBA's 50 lead TSOP II 50-P-400 device (64 Mb synchronous DRAM) as the baseline for numerical modeling (see Fig. 1). Three cases have been simulated under the random vibration testing conditions specified in NASA GSFC's small payload and sub-system test guidelines [2]:

1. Large chip (10.0 mm x 20.0 mm x 0.8 mm)

2. Small chip (1.6 mm x 1.0 mm x 0.6 mm)

3. Medium chip (4.0 mm x 15.0 mm x 0.5 mm)

Dynamic modal analysis and random vibration analysis are performed for all three cases to compare the resonant frequencies as well as dynamic stresses.

2. FEA MODEL

Fig. 2 shows the FEA model for this TSOP device (enlarged local view for the device). A very fine FEA mesh is utilized for the leads and solder joints for improved resolution. This model consists of 23388 3-D 8-node elements. The PCB dimension is 4.5" x 4.5" x 0.062".

3. MATERIAL PROPERTIES

Table 1 lists the room-temperature material properties used in this study:

Table 1

MATERIAL	Si	Fe/Ni Alloy	Solder	FR-4	Molding Compound
YOUNG'S MODULUS(Gpa)	110	145	14.9	17	31
POISSON'S RATIO	0.28	0.3	0.29	0.3	0.22
DENSITY (kg/m^3)	2330	8110	8470	1938	2014

4. BOUNDARY CONDITIONS AND ACCELERATION SPECTRAL DENSITY

The boundary conditions in the simulation are reflecting the vibration testing fixtures used in the GSFC technology assurance labs. Four screws are used at the four corners of the PCB to rigidly mount the board onto the vibration shaker, providing complete restraint in Dx, Dy, and Dz movements.

The input acceleration spectral density (ASD) for this simulation is specified by NASA GSFC for most electronic sub-systems. This ASD is shown in Fig. 3.

5. MODAL RESULTS

Figs. 4-7 show the first four resonant modes for the "large chip" case. The resonant frequencies are:

F1 = 612 Hz

F2 = 1237 Hz

F3 = 1241 Hz

F4 = 1499 Hz

As a comparison, we also obtained the first four resonant modes for the case of the "small chip". The results are:

F1 = 612 Hz

F2 = 1237 Hz

F3 = 1240 Hz

F4 = 1495 Hz

One can see that the impact of the different chip size is indeed minimum, because the major vibrational mass is the PCB.

6. DYNAMIC STRESS RESULTS

In the dynamic stress analysis, our interest is in finding out the root-mean-square (RMS) stress on the body of silicon material at the first resonance, namely, 612 Hz, as this mode has typically has the largest displacements and therefore the highest dynamic stresses. Figs. 8, 9, and 10 show the RMS maximum principal stress distributions in the silicon material for a large chip, a medium chip and a small chip respectively. The results are summarized in Table 2.

Table 2.

	LARGE CHIP	MEDIUM CHIP	SMALL CHIP
FIRST RESONANT FREQUENCY (Hz)	612	612	612
MAXIMUM PRINCIPAL STRESS (3σ RMS) (Pa)	2.46×10^{-4}	8.25×10^{-6}	2.36×10^{-6}
RATIO BASED ON SMALL CHIP CASE	104.2	3.5	1.0

From Table 2, we can see that the maximum principal stress at 612 Hz in the silicon differs significantly with the chip size. The difference between the small and large chips is as much as two orders of magnitude. The dynamic effect of stress distribution in the silicon is indeed highly significant.

However, due to the extremely low profile and small mass of this TSOP device, the actual values of dynamic stresses are very low, and will not cause any concern in terms of the integrity of the silicon material. In reality, silicon shall be safe if the stress in the material is under 30 MPa, although test data have been reported that silicon can fracture at 19 MPa if the surface of the material is very rough.

7. SUMMARY

Dynamic stress analyses have been performed for the TOSHIBA DRAM TSOP 50-lead device for the purposes of understanding the dynamic impact of vibration on silicon chips a relative sizes. FEA results have convincingly revealed that the dynamic impact due to variation of size of the silicon is very significant, which confirmed our original thoughts about the size of the chip and its dynamic responses. However, because of its extremely low profile and low mass, the absolute values of dynamic stresses are insignificant and will by no means cause any harm to the silicon chip inside the TSOP device. Thus, in selecting TSOP devices with chip-size variations, we shall have no concern about whether the chip is too large. However, this conclusion is only valid for

very low profile TSOP devices. If a PEM device is not the TSOP type, then chip-size variation may have significant dynamic impact. Under these circumstances, the dynamic impact of chip size shall be evaluated on a case-by-case basis.

8. REFERENCES

[1] Mark S. Fan and Gregory L. Rose, "Transient Thermal and Stress Analysis for TSOP Devices", in "1997 International Symposium on Microelectronics", pp. 290—295.

[2] "General Environmental Verification Specification for STS & ELV Payloads, Subsystems, and Components", NASA GSFC, Jan. 1990.

TSOP II 50-P-400-0.80D

Unit : mm

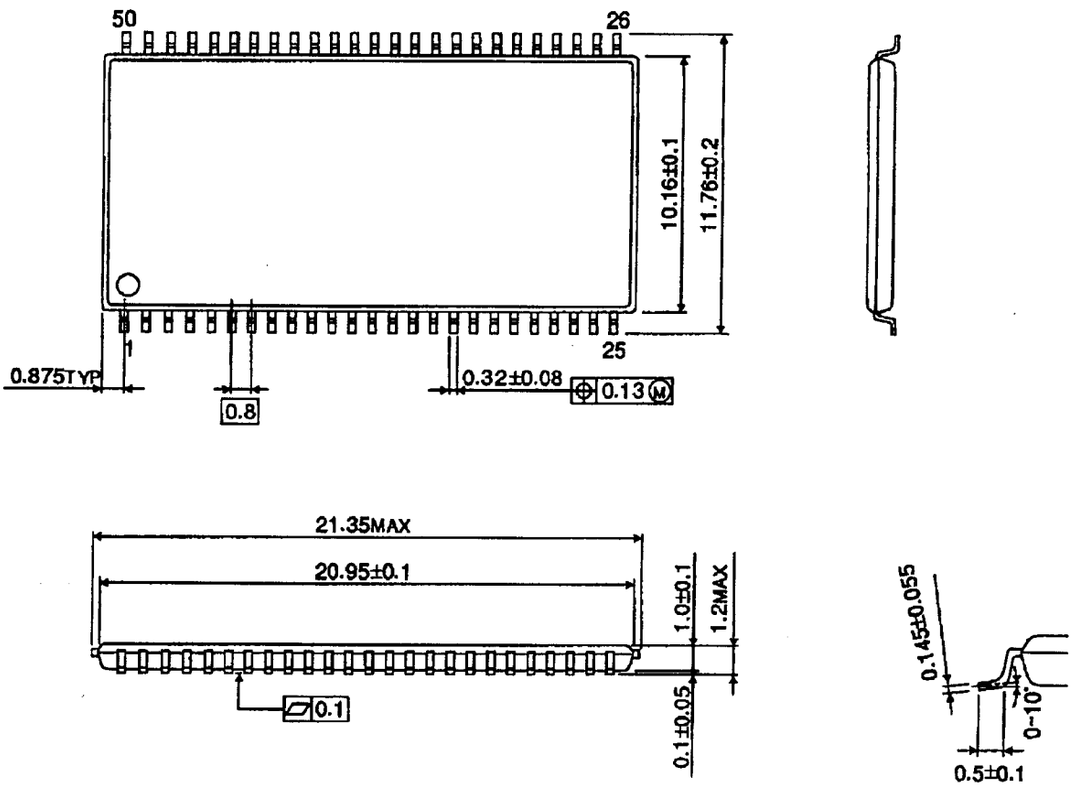


Fig. 1

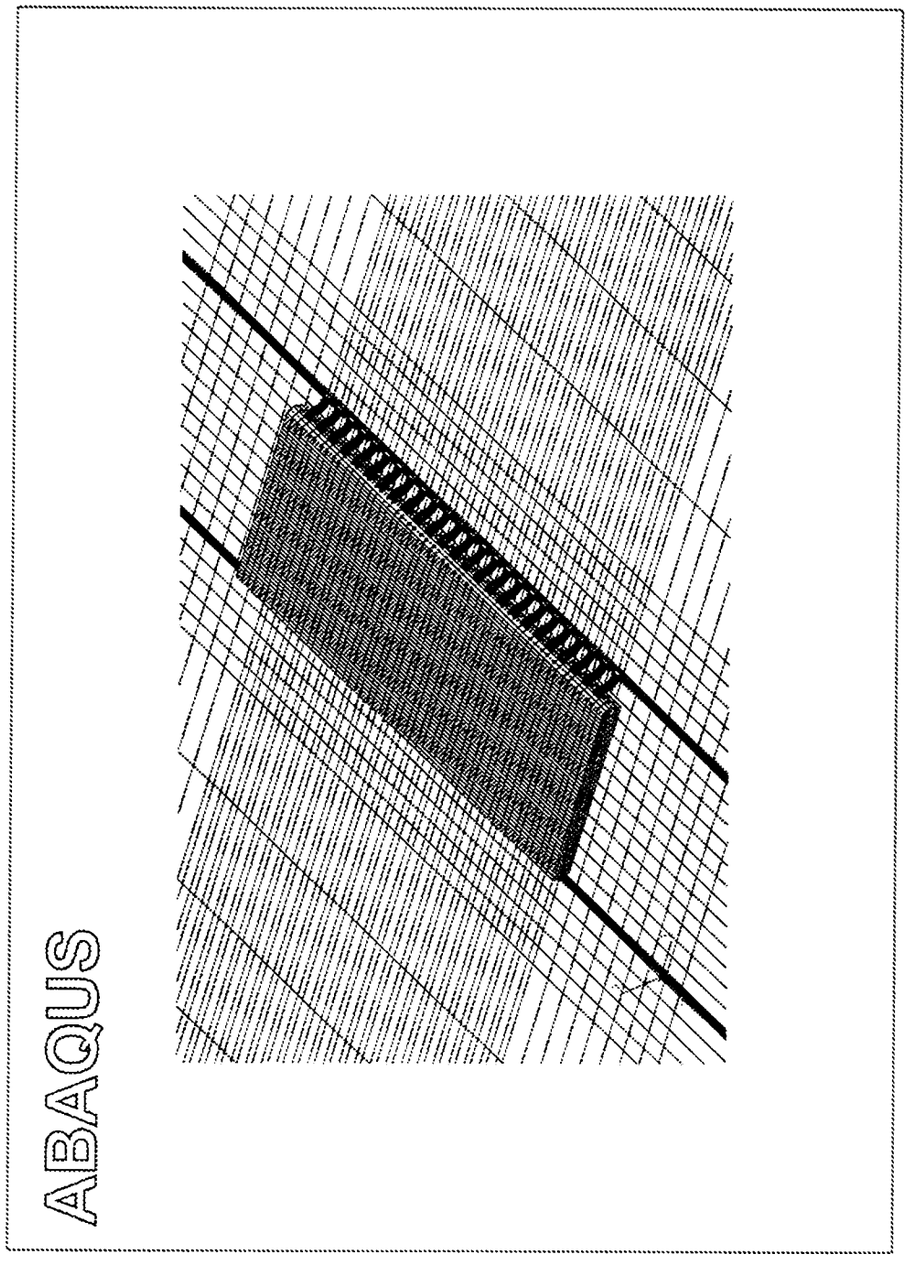
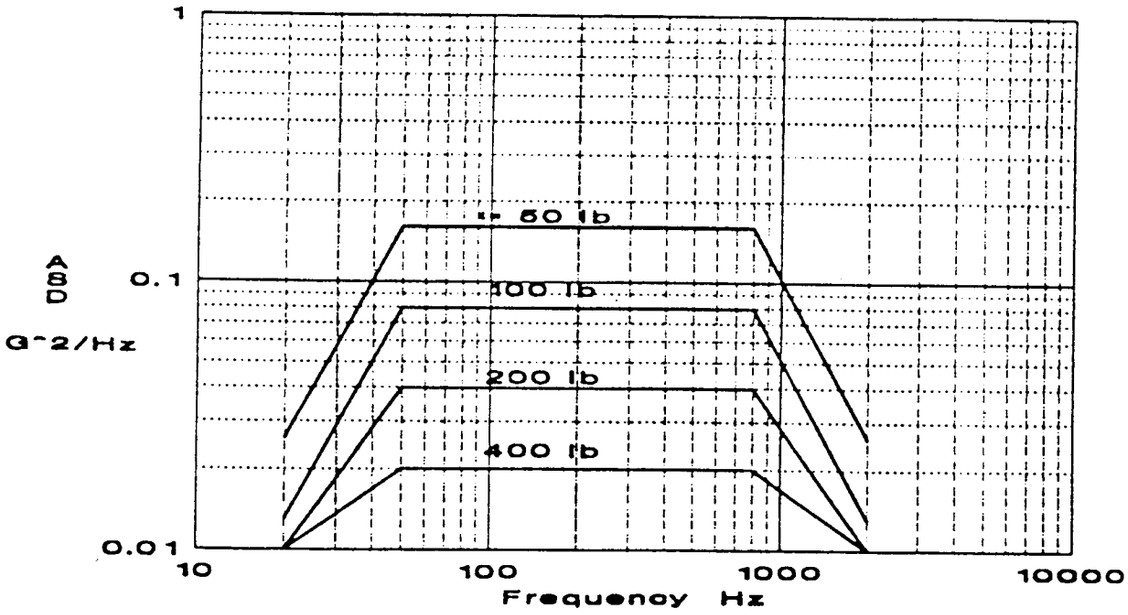


Fig. 2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Frequency Hz

Fig. 3

Fig. 4

Fig. 4

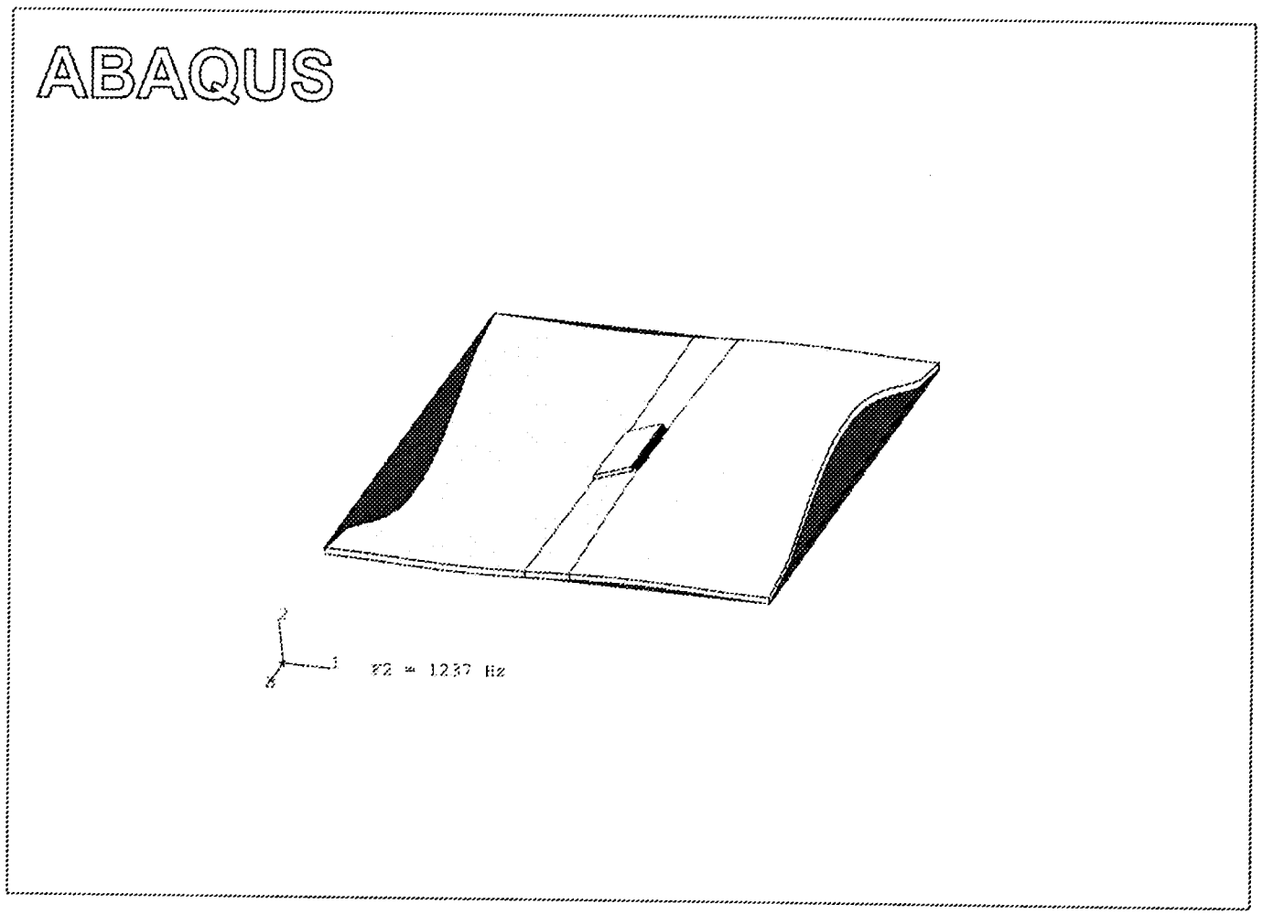
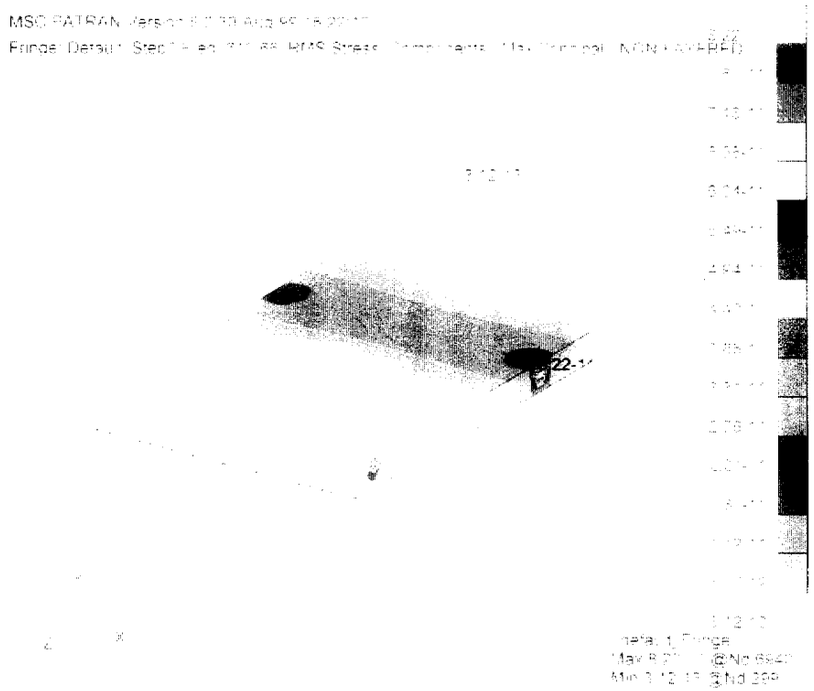


Fig. 5

Fig. 6.

Fig. 7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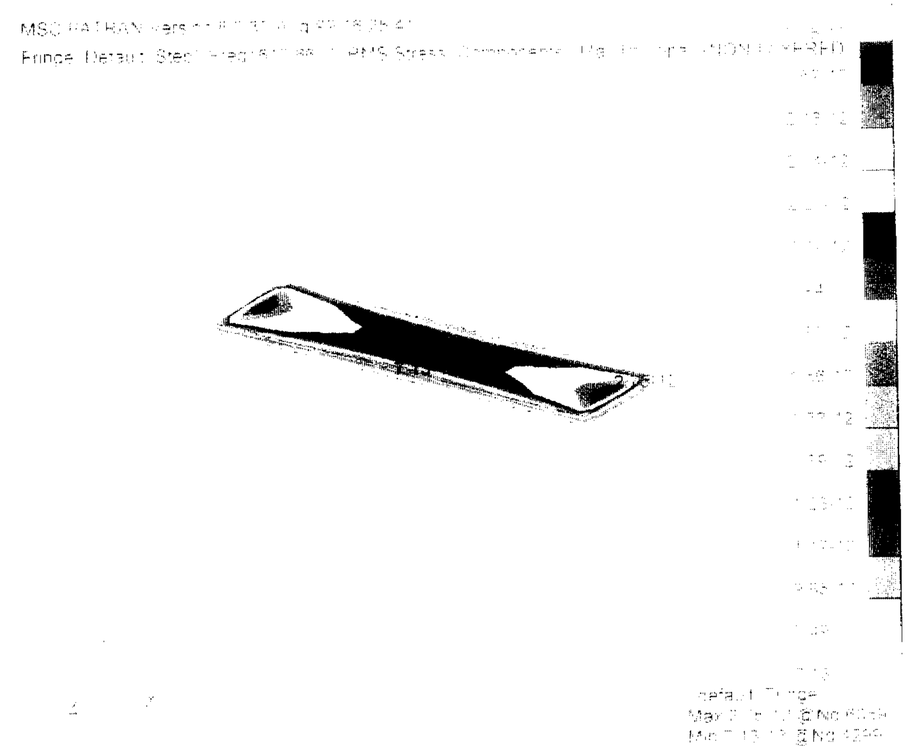
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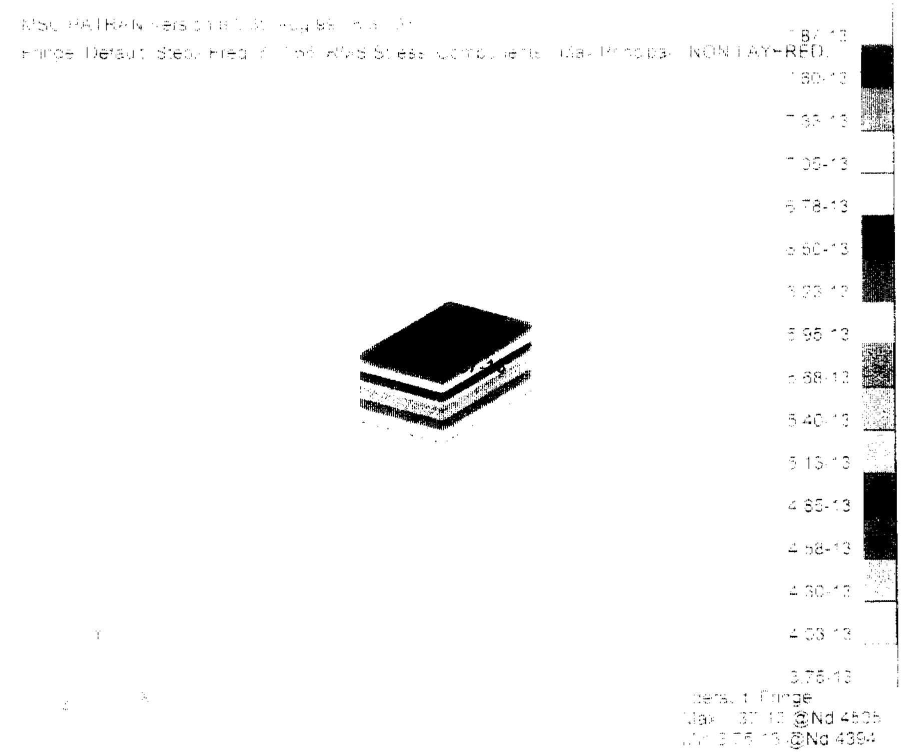
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